Scheme and Syllabus
M. Tech (VLSI Design & Embedded system)
Batch 2016 onwards
Vision of BMS College of Engineering

*Promoting Prosperity of mankind by augmenting human resource capital through Quality Technical Education & Training*

Mission of BMS College of Engineering

*Accomplish excellence in the field of Technical Education through Education, Research and Service needs of society*

Vision of Electronics and Communication Department

*To emerge as a Centre of Academic Excellence in Electronics, Communication and related domains through Knowledge acquisition and Knowledge dissemination meeting the global needs and standards.*

Mission of Electronics and Communication Department

*Imparting quality education through state of the art curriculum, conducive learning environment and Research with scope for continuous improvement leading to overall Professional Success.*

Web: [www.bmsce.ac.in](http://www.bmsce.ac.in)

**PROGRAM EDUCATIONAL OBJECTIVES**

**PEO1:**
Graduates shall be capable of building their career in related industries, R&D establishments as well as in Teaching with their scholarly knowledge with respect to advanced topics in VLSI Design & Embedded system

**PEO-2:**
Graduates shall be capable of conceptualizing and analysing engineering problems of societal importance related to Design, implement, verification of Integrated circuit and embedded system, conduct independent research leading to technology solutions and communicate the outcomes through verbal and written mechanisms.

**PEO-3:**
Graduates shall be able to collaborate, manage and execute projects in teams using appropriate tools/technologies with utmost professionalism and acceptable good practices.
PROGRAM OUTCOMES
Program Outcomes (POs), are attributes acquired by the student at the time of graduation. The POs are aligned to the Graduate Attributes (GAs) specified by National Board of Accreditation (NBA). These attributes are measured at the time of Graduation, and hence computed every year for the outgoing Batch. The POs are addressed and attained through the Course Outcomes (COs) of various courses of the curriculum.

PO1: Acquire scholarly knowledge beginning with fundamentals up to the global perspective.

PO2: Think critically, and shall be able to plan and conduct research oriented experiments along with collection and analysis of results.

PO3: Conceptualize and solve contemporary engineering problems and propose optimal solutions in core and related areas.

PO4: Acquire necessary research skills and contribute individually/in group(s) to the development of technology in his/her core area of expertise.

PO5: To select, learn and apply appropriate techniques, resources, and modern engineering and IT tools in his/her core area and allied areas.

PO6: Collaborate and develop a capacity for self-management and team work.

PO7: Manage and execute projects efficiently at engineering, financial and personnel levels.

PO8: Demonstrate effective verbal and written communication skills, in the form of technical documentation, presentations, standards compliance etc.

PO9: Recognize the need for, and have the preparation and ability to engage in life-long learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

PO10: Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO11: Observe and examine critically the outcomes of one’s actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback.
Total Number of Credits (I Sem – IV Sem) = 100 Credits

<table>
<thead>
<tr>
<th>Category</th>
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<tr>
<td>Program Core Course</td>
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<td>Project Work</td>
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Distribution of credits

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Distribution of self-study components:

Note: Self-Study components is provided for the DCC
## M.Tech. (VLSI Design and Embedded system)

### I Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Course Title</th>
<th>Credits</th>
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<tbody>
<tr>
<td>16ECVEPCAM</td>
<td>Advanced Mathematics</td>
<td>3</td>
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<tr>
<td>16ECEVEGCDV / 16ECELGEDV</td>
<td>Digital VLSI design</td>
<td>3</td>
</tr>
<tr>
<td>16ECEVEGCES / 16ECELGCES</td>
<td>Advanced Embedded system</td>
<td>3</td>
</tr>
<tr>
<td>16ECVEPCAI</td>
<td>Analog IC design</td>
<td>3</td>
</tr>
<tr>
<td>16ECEVEPEZZ</td>
<td>Elective -1</td>
<td>3</td>
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<tr>
<td>16ECEVEPEZZ</td>
<td>Elective -2</td>
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<td>16APRDICRM</td>
<td>Research Methodology</td>
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**Total** 20 1 2 2 25

**Note:** Two electives to be chosen from the list below:
Elective will be offered for a minimum strength of six candidates (out of 18) / eight candidates (out of 24)

### Course Elective

<table>
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<th>Subject Code</th>
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<td>16ECVEPELP</td>
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<td>16ECVEPEEC</td>
<td>Embedded C</td>
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<td>16ECVEPEST</td>
<td>Static Timing Analysis</td>
<td>16ECVEPEAV</td>
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<tr>
<td>16ECVEPEEMP</td>
<td>Device Modeling and Processing Technology</td>
<td>16ECVEPESP</td>
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Note: (i) The Course Code Expansion: Exa: 16ECVEPCAM: 16 = Year, EC = Dept., VE = Program, PC = Program Core, AM = Advanced Mathematics.

ZZ(course abbreviation), GC/GE: Group Core / Group Elective

(ii) Exception for 16APRDICRM: AP = All Program, RD = Research & Development, I = Institution C = Core, RM = Research Methodology.

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### M.Tech. (VLSI Design and Embedded system)  
#### II Semester  
#### CREDIT BASED

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<tr>
<th>Subject Code</th>
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**Note:** Two electives to be chosen from the list below:  
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<table>
<thead>
<tr>
<th>Course Elective</th>
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<tbody>
<tr>
<td>16ECVEPESV System Verilog and verification</td>
<td>16ECVEPEHS Hardware/Software Co-design</td>
</tr>
<tr>
<td>16ECVEPEPD Physical Design</td>
<td>16ECVEPEAM Embedded Design using ARM Architecture</td>
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### M.Tech. (VLSI Design and Embedded system)

#### III Semester

<table>
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<td>Internship</td>
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<td>16ECVEPCIP</td>
<td>Project work (I-phase)</td>
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<td><strong>Total</strong></td>
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**NOTE:**

**III Semester:**

- **Internship:** The student shall undergo internship for 16 weeks.
- **Preliminary Report** submission and Evaluation after 8th week of Internship to be carried out by the Internal Guide of the college and a senior faculty for **100 marks**
- **Final Report** submission and Evaluation after 16th week of Internship to be carried out by the Internal Guide of the college and a senior faculty. Report Evaluation to be completed within two weeks of submission for **100 marks**.

**Viva-Voce on Internship** - To be conducted by the Internship Guide (from the college) and the External Guide / Examiner within 2 weeks of Submission with a senior faculty / HoD as chairman for **100 marks**

- **Project Phase: I**

**Problem formulation** and submission of **synopsis** within 8 weeks from the commencement of 3rd semester, which shall be evaluated for **50 marks** by the committee constituted for the purpose by the Head of the Department comprising the guide, senior faculty of the department with HoD as Chairman.

**Literature survey and progress** done after 16 weeks shall be evaluated by guide and external examiner with senior faculty / HoD as chairman for **50 marks**
M.Tech. (VLSI Design and Embedded system)

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Course Title</th>
<th>Credits</th>
<th>CREDITS</th>
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<td>Project work (final phases)</td>
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<td>16 ECVEPCTS</td>
<td>Technical Seminar</td>
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<td>Total</td>
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</table>

IV Semester:

- **Project Phase-II** - Internal Evaluation of progress in Project work shall be evaluated after 8 weeks for 100 marks by the committee constituted for the purpose by the Head of the Department comprising the guide and senior faculty of the department with HoD as Chairman.

- **Project Phase-III** - Internal Evaluation of Project Demonstration, which shall be evaluated after 15 weeks for 100 marks by the committee constituted for the purpose by the Head of the Department.

- **Final Evaluation of Project Work and Viva-voce.**
  - Final evaluation of project to be carried out after 16 weeks from the date of commencement of 4th semester.
  - The Internal Examiner (the project guide with a teaching experience of at least three years) and External Examiner with HoD as chairman will complete the final evaluation of Project.

- Internal and External Examiners shall carry out the evaluation for 100 Marks each and the average of these marks shall be the final marks of the Project Evaluation.

- **Viva – Voce** : The Viva-Voce shall be conducted jointly by Internal Examiner and External Examiner with HoD as chairman for **100 Marks**.
Advanced Mathematics

<table>
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<th>COURSE TITLE</th>
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<table>
<thead>
<tr>
<th>CO-No</th>
<th>Course Outcomes</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO-1</td>
<td><strong>Demonstrate</strong> an understanding to multiple random variables, vector spaces, linear transformations and inner product spaces and <strong>Apply</strong> probability techniques to determine the mutual information in a communication channel and Apply various algorithms in graph theory to solve networking and communication problems.</td>
</tr>
<tr>
<td>CO-2</td>
<td><strong>Analyse</strong> the random process for SSS, WSS, and ergodic in the mean or ergodic in the autocorrelation.</td>
</tr>
<tr>
<td>CO-3</td>
<td><strong>Construct</strong> the Singular value decomposition of a matrix A.</td>
</tr>
<tr>
<td>CO-4</td>
<td><strong>Conduct</strong> numerical experiments with matlab in Gram-Schmidt orthogonalisation process, advanced matrix theory and graph theory and <strong>Make an effective oral presentation</strong> of the applications of random variables, random processes, vector spaces and network flow algorithms</td>
</tr>
</tbody>
</table>

**Pre-requisites:** Basic concepts of Probability, Bayes’ theorem. Vector algebra, matrix operations.

**Random Variables:** Discrete and continuous type Random Variables, Sequence of random variables, limit theorem, random correlation function, spectral densities, linear systems with random inputs, Distribution and Density Functions: PMF, CDF, PDF, Gaussian random variable, and other standard random variables, Expectation operator, Multiple random variables: Joint PMF, CDF, PDF, Expectation involving multiple Random variables.

**Vector Spaces and subspaces:** Vector spaces, basis and dimension, linear transformations, inner product spaces orthonormal bases and Gram-Schmidt orthogonalisation process.

**Advanced Matrix Theory:** Introduction to eigenvalues and eigenvectors, Positive definite matrices, Singular value decomposition, Principal component analysis by SVD, geometry of SVD - Least square approximations.

**Computational Graph Theory:** Graph enumerations and optimization: DFS-BFS algorithm, shortest path algorithm, min-spanning tree and max-spanning tree algorithm, basics of minimum cost spanning trees, optimal routing trees, optimal communication trees, planarity algorithm, Fundamental algorithmic techniques for solving graph problems-Traversal and search techniques, Greedy approach, Backtracking, Branch and bound techniques and their applications to various graph problems, Network flow algorithms, Classification of graph problems P, NP-hard and NP-complete.

**Text Books:**

**Reference books:**
3. MIT Open courseware, Introduction to Linear Algebra, Course 18.06
4Nausing Deo, “Graph Theory with applications to Engineering and Computer Science”, Prentice Hall of India, 1999.

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**Digital VLSI Design**

<table>
<thead>
<tr>
<th>COURSE CODE</th>
<th>16ECVEPCDV/16ECELGEDV</th>
<th>COURSE TITLE</th>
<th>Digital VLSI Design</th>
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<td>CREIDTS</td>
<td>4</td>
<td>L-T-P-S</td>
<td>3-1-0-0</td>
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</table>

**CO1** Apply the concepts of MOS system in digital VLSI design
**Department of Electronics & Communication Engineering**

| CO2 | **Analyse** the electrical and physical properties, Switching characteristics and interconnect effect of a MOS system in digital VLSI design |
| CO3 | **Design** dynamic logic circuits, Semiconductors Memory circuits, and different CMOS logic circuits. |
| CO4 | Use **modern tools** to simulate Schematic and Layout of Digital circuits individually/ in group (s) and Make an **effective oral presentation** and documentation on advanced topics related to the course by referring IEEE Journals. |

**MOS Transistor:** The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **Layout and stick diagrams**

**MOS Inverters:** Static Characteristics: Resistive load inverters, CMOS Inverter.

**Switching Characteristics and Interconnect Effects:** Delay-Time Definition, Calculation, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitic, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.


**Semiconductor Memories:** Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM).

**Reference Books**


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**Advanced Embedded Systems**

<table>
<thead>
<tr>
<th>COURSE CODE</th>
<th>16ECVEGCES / 16ECELGCES</th>
<th>COURSE TITLE</th>
<th>Advanced Embedded Systems</th>
</tr>
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<tbody>
<tr>
<td>CREIDTS</td>
<td>5</td>
<td>L-T-P-S</td>
<td>3-0-1-1</td>
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**CO-No**

**Course Outcomes**

<p>| CO-1 | Understand and explain the concepts of Embedded Systems and <strong>Apply</strong> the knowledge of Computer Architecture in <strong>building</strong> Embedded Systems. |
| CO-2 | <strong>Analyze</strong> the real-time deterministic response of embedded systems and various peripherals involved in <strong>Embedded</strong> system. |</p>
<table>
<thead>
<tr>
<th>CO-3</th>
<th><strong>Design</strong> low power, real time deterministic Embedded Systems and <strong>Develop C programs, execute &amp; demonstrate</strong> on embedded target boards like Beagle Bone Black, Raspberry Pi, Arduino, etc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO-4</td>
<td><strong>Perform in a team</strong> to design and develop useful embedded systems and Make an <strong>effective oral presentation</strong> on topics allocated by instructor pertaining to Computer Architecture, Embedded Systems, Analog and Digital peripherals.</td>
</tr>
</tbody>
</table>

**Introduction to Embedded Systems**, Real time nature of ES, Architectures of ES including multi core architecture, Graphic Processing Units (GPU), Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components. **Case Study Raspberry Pi 3**.


**USB Basics**, Uses and limits, Benefits, Evolution, Bus components, Division of labor, Transfer basics, Elements of a transfer, USB 2.0 transactions, Ensuring successful transfers, Control transfers, Bulk transfers, Interrupt transfers, Isochronous transfers, Enumeration: Process and Descriptors.


**Lab Experiments:**

1. Raspberry Pi 3: Booting the Board with multiple OS, Programming of GPIO, Programming of Serial Peripherals, Control of ADC.

2. Zynq Board: Implement Timers and GPIO modules in FPGA and control it with ARM SOC.

3. Implement a USB generic serial emulator device on FPGA, interface it with Raspberry Pi 3.

**Reference Books:**

3. The Zynq Book, by Crockett, Elliot, Enderwitz & Stewart, University of Strathclyde Glasgow, 2014
4. USB Complete: The Developer's Guide, Jan Axelson

Analog IC design

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<table>
<thead>
<tr>
<th>CO-No</th>
<th>Course Outcomes of Analog ic design</th>
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<tbody>
<tr>
<td>CO-1</td>
<td>Understand and explain Basic physics and operation of MOS devices and apply the knowledge of Network theory, Electronic circuit design, VLSI design to obtain Analog design actagon.</td>
</tr>
<tr>
<td>CO-2</td>
<td>Analyse the Analog circuits by developing efficient analytical tools for quantifying the circuits by inspection.</td>
</tr>
<tr>
<td>CO-3</td>
<td>Design stable Analog Integrated Circuits to meet given specification</td>
</tr>
<tr>
<td>CO-4</td>
<td>Conduct Research based experiments to demonstrate optimized Analog Integrated Circuit design by suitable literature survey and suitable EDA Tool (Cadence, Synopsis, Mentor graphics)</td>
</tr>
<tr>
<td>CO-5</td>
<td>Involve in independent/team learning, Communicate effectively and engage in life-long learning</td>
</tr>
</tbody>
</table>

Basics of MOSFET, MOS I/V Characteristics, second order effects, MOS device models.

Single stage Amplifier: CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source Degeneration, source follower, common-gate stage, cascade stage, choice of device models.

Differential Amplifiers & Current Mirrors: Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell.
Basic current mirrors, Cascade mirrors, active current mirrors.


**Band Gap Reference Design:** General considerations, Supply independent biasing, temperature independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, constant gm biasing

**Lab Experiments:**
1. **Design the analog circuits using MOS transistors,**
a. Draw the schematic and verify the following
   (i) DC Analysis
   (ii) AC Analysis
   (iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS.

2. **Design, an op-amp with given specification using given differential amplifier in library and complete the design flow mentioned below:**
a. Draw the schematic and verify the following
   (i) DC Analysis
   (ii) AC Analysis
   (iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC

**Reference Book:**
I Semester electives
Advanced Digital logic Design

<table>
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<thead>
<tr>
<th>CO</th>
<th>Course Outcomes</th>
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<tbody>
<tr>
<td>CO-1</td>
<td>Apply the concepts of Digital design to create digital building blocks using Verilog.</td>
</tr>
<tr>
<td>CO-2</td>
<td>Analyse the RTL timing to report violations and synthesize to generate gate level net list.</td>
</tr>
<tr>
<td>CO-3</td>
<td>Design of RTL using finite state machines along with design optimization.</td>
</tr>
<tr>
<td>CO-4</td>
<td>Simulate and debug the design using test benches and analyse the synthesis timing and power reports using modern tools.</td>
</tr>
</tbody>
</table>


Synthesis, Libraries and Technology Mapping: Introduction to synthesis, logical synthesis of basic combinational and sequential circuits, Synthesis Methodologies, Pre and post synthesis mismatch, Translation, mapping and optimization. Overview of Libraries, design constraints, importance of wire load models.

Design and simulation of Architectural building blocks: Basic Building blocks design using Verilog HDL: Arithmetic Components – Adder, Subtractor, and Multiplier design, Data Integrity – Parity Generation circuits, Control logic – Arbitration schemes, FSM Design – overlapping and non-overlapping Mealy and Moore state machine design.

Verification Concepts: Concepts of verification, importance of verification, Types of verification (black, white and gray box verification), Stimulus vs Verification, functional verification, functional verification approaches, typical verification flow, directed and random verification, Coverage: Code and Functional coverage, Coverage driven verification.

Reference Books:
3. *Verilog HDL Synthesis A Practical Primer* by J. Bhasker

Embedded C

<table>
<thead>
<tr>
<th>COURSE CODE</th>
<th>16ECVEPEEC</th>
<th>COURSE TITLE</th>
<th>Embedded C</th>
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<tbody>
<tr>
<td>CREIDTS</td>
<td>3</td>
<td>L-T-P-S</td>
<td>3-0-0-0</td>
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</table>

CO1 Understand the syntax and semantic of the C language for embedded programming and various Inter Process Communication mechanism.

CO2 Apply C Features to develop Embedded C.

CO3 Analyse various usage of pointer, user defined types in C programming.

CO4 Develop multitasking and multithreading programming.

Quick Overview of C: C Features, Application of C, Build Process, Scope of a variable, Storage Class, operators, Condition statement, Memory layout of C program

User Define Data type: Arrays, Structures, Union, enum.

Purpose of Pointers: Need for pointers, Pointer to built in type, Pointer to user defined type, Command line arguments, Dynamic memory allocation, Function pointer, call back functions, pointer to pointer, Memory mapping.

Functions and C Pre-processor Directives: using built in function/library, user defined functions, Developing Static Library and Dynamic Library.
**File I/O:** Formatted I/O, system I/O, treatment of devices as files in Posix, File I/O in Windows, fopen, fwrite, fread, fclose, fprintf, fscanf, open, read, write, close, & ioctl calls

**Multitasking using Process and Thread:** Process creation, Process termination, Thread creation and termination,

**Inter Process Communication:** Signals, Pipe, FIFO, Message Queue, Shared Memory, Semaphores

**References:**
1. The C Programming: Brian W Kernighan, Dennis M Ritchie
2. Understand Pointer in C: Yeshavanth Kanetkar
3. Linux System Programming: Robert Love

### Device Modeling and Processing Technology

<table>
<thead>
<tr>
<th>COURSE CODE</th>
<th>16ECVEPEMP</th>
<th>COURSE TITLE</th>
<th>Device Modeling and Processing Technology</th>
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<td>L-T-P-S</td>
<td>3-0-0-0</td>
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**CO**
Course Outcomes

**CO-1**
Understand fundamentals of semiconductors, theoretical and practical aspects of electronics technology – Very Large Scale Integration. All the unit process steps involved in planar process starting from silicon crystal growth to CMOS Process.

**CO-2**
Analyse SPICE Models of Diodes, BJT, MOSFETs, MESFETs & HBTs.

**CO-3**
Ability to submit a report on the SPICE models fabrication process

**Fundamentals:** Semiconductor Physics, Principle of circuit simulation and its objectives.

**Introduction to SPICE:** AC, DC, Transient, Noise, Temperature extra analysis.

**Junction Diodes:** DC, Small signal, large signal, High frequency and noise models of diodes, Measurement of diode model-parameters.

**Modelling of BJT:** DC, small signal, high frequency and noise models of bipolar junction transistors. Extraction of BJT model parameters.

**MOSFETs:** DC, small signal, high frequency and noise models of MOSFETs, MOS Capacitors. MOS
**Models:** Level-1 and level-2 large signal MOSFET models. Introduction to BSIM models. Extraction of MOSFET model parameters.

**JFET, MESFETs & HBTs:** Modelling of JFET & MESFET and extraction of parameters. Principles of hetero-junction devices, HBTs, HEMT.


<table>
<thead>
<tr>
<th>CO-NO</th>
<th>Description</th>
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<tbody>
<tr>
<td>CO1</td>
<td>Apply the learnt basic concepts of STA to evaluate the delay of the circuits.</td>
</tr>
<tr>
<td>CO2</td>
<td>Analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing.</td>
</tr>
</tbody>
</table>

**Text Books**


**References**

1. Sedra and Smith, SPICE.
2. H.M. Rashid, Introduction to PSPICE, PHI.
3. B.G. Streetman & S. Baneerjee, Solid State Electronic Devices, PHI.
4. R. Raghuram, Computer Simulation of Electronic Circuits, Wiley Eastern Ltd.

**Static Timing Analysis**

<table>
<thead>
<tr>
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<th>COURSE TITLE</th>
<th>Static Timing Analysis</th>
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18
Static Timing Analysis Concepts: Propagation delay, slew, timing arcs, min and max timing paths, clock domains.
Standard Cell Library: Pin capacitance, timing models: linear v/s. non-linear delay model, combinational v/s. sequential cells, state-dependent models, models for crosstalk and noise, characterization.
Interconnect Parasitic: RLC modelling, wire load models, representation of coupling capacitances, reducing parasitic for critical nets.
Delay Calculation: Basics, delay calculation with interconnect, calculation at pre- and post-layout stages, calculation using effective capacitance, interconnect delay, slew merging, path delay calculation, slack calculation
Crosstalk and Noise: Crosstalk glitch analysis, crosstalk delay analysis, setup and hold analysis.
The STA Environment: timing path groups, modelling of external attributes, virtual clocks, refining the timing analysis, point-to-point specification.
Timing Verification: Setup and Hold timing checks, recovery and removal checks, multi-cycle paths, false paths, timing across clock domains.
Robust Verification: on-chip variations, time borrowing, clock gating checks, sign-off methodology, Best case (BCS) Typical(Typ) and Worstcase(WCS) corners. statistical static timing analysis

References:
3. Research papers

Low Power VLSI

<table>
<thead>
<tr>
<th>COURSE CODE</th>
<th>16ECVEPELP/ 16ECELPELP</th>
<th>COURSE TITLE</th>
<th>Low Power VLSI</th>
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</table>

Supply Voltage Scaling Approaches: Device feature size scaling Multi-Vdd Circuits Architectural level approaches: Parallelism, Pipelining Voltage scaling using high-level transformations Dynamic voltage scaling Power Management

Switched Capacitance Minimization Approaches: Hardware Software Tradeoff Bus Encoding Two’s complements Vs Sign Magnitude Architectural optimization Clock Gating Logic styles

Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach Multi-threshold-voltage CMOS (MTCMOS) approach Power gating Transistor stacking Dual-Vt assignment approach (DTCMOS)

Special Topics: Adiabatic Switching Circuits Battery-aware Synthesis Variation tolerant design CAD tools for low power synthesis

Text

Reference
2. NPTEL http://nptel.iitm.ac.in Computer Science and Engineering, Department of Computer Science and Engineering, IIT Kharagpur

Embedded Computing and networking
**COURSE CODE**: 16ECVEPEEC  
**COURSE TITLE**: Embedded Computing and networking  
**CREDITS**: 3  
**L-T-P-S**: 3-0-0-0

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<tbody>
<tr>
<td>CO1</td>
<td>Understand different types of Embedded Applications.</td>
</tr>
<tr>
<td>CO2</td>
<td>Analyse various development tools, WAN, LAN and PAN protocols</td>
</tr>
<tr>
<td>CO3</td>
<td>Customize Linux for different environment</td>
</tr>
<tr>
<td>CO4</td>
<td>Port OS to embedded board and to build Arm tool Chain</td>
</tr>
</tbody>
</table>

**Types of embedded application**: Super loop, Interrupt driven, priority, round robin, OS based.

**Embedded Android**: Android Mobile and Tablet, Android TV, Android Wearable, Android Auto, Glass.

**WAN**: MPLS, HTTP, MQTT, Coap etc.

**LAN**: TCP / IP, UDP, Socket Programming

**PAN**: Bluetooth, BLE, zigbee

**Introduction to Software Development Tools**: GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

**Interfacing Modules**: Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

**Building an Embedded System**: Creating the Root File system, Building the Linux Kernel, Building the Root File system, Running UML, Networking.

**Embedded ARM Devices**: Building ARM tool chain, Installing an Operating System on ARM board, Using ARM board Serial Port, Remote Serial Port.

**Text books**:  
3. Assembly Language for x86 Processors by Kip R. Irvine  
4. Embedded Operating System - Alan Holt, Chi-Yu Huang, Springer  
5. Intel® 64 and IA-32 Architectures Software Developer Manuals

**Reference books**:  
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall  
3. UNIX Network Programming by W. Richard Stevens


**Advances in VLSI Structure**

<table>
<thead>
<tr>
<th>COURSE CODE</th>
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<th>COURSE TITLE</th>
<th>Advances in VLSI Structure</th>
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<th>CO</th>
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<tbody>
<tr>
<td>CO1</td>
<td>Ability to understand multiple-gate MOSFET’s. Strained-Si technology, thin body MOSFET’s and Emerging nano materials</td>
</tr>
<tr>
<td>CO2</td>
<td>Apply the short channel effect to define new structures and requirement of new materials</td>
</tr>
<tr>
<td>CO3</td>
<td>Analyse thin body MOSFET structure and its impact, Impacts of substrate; nano materials</td>
</tr>
<tr>
<td>CO4</td>
<td>Use modern tool to simulate different structure and observe the performance comparison</td>
</tr>
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</table>

**Transistor and multiple-gate MOSFET’s**

development, history, review of MOSFET principles and performance metrics

**Issues in short-channel MOSFET**
electrostatics; scale length fundamentals for thin-body MOSFETs (FinFET, planar Fully-Depleted SOI MOSFET and Gate-All-Around MOSFET)

**Advantages of thin body MOSFET’s**
electrostatics quantum mechanical effects; effective carrier mobility; high-field velocities. Parasite resistance; thin-body MOSFET’s carrier transport MOSFET compact modelling and Technology CAD (TCAD)

**Impacts of substrate:**

Fin shape tuning; Gate stack process, FinFET’s source/drain process, Multiple-gate MOSFET’s threshold voltage engineering. Multiple-gate MOSFET performance dependence on channel orientation and strain

Strained-Si technology and its effectiveness on Multiple-gate MOSFETs high-mobility channel transistors (Group III-V)

Emerging nano materials: Nanotubes, nanorods and other nano structures, MOSFET like structure of carbon nano tubes.

**Reference:**

1. Research papers
2. MOOC: http://www.flexilearn.ie/course/Nanoelectronics/43

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**VLSI Signal Processing**

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<th>COURSE TITLE</th>
<th>VLSI Signal Processing</th>
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**CO** | **Description**  
---|---  
**CO1** | Understand Pipelining architecture and parallel processing of FIR filters, Fast convolution algorithms for IIR filters  
**CO2** | Analyse Retiming folding and unfolding algorithms and implement into the different FIR filters, Fast convolution algorithms for IIR filters.  
**CO3** | Implementing algorithms into different architectures and synchronous, asynchronous systems  

**Introduction to DSP systems, pipelining and parallel processing of FIR filters:** Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.


**Fast convolution, pipelining and parallel processing of IIR filters:** Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

**Bit-level arithmetic architectures:** Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

**Numerical strength reduction, synchronous, wave and asynchronous pipelining:** Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

**References:**

**RESEARCH METHODOLOGY**

**COMPULSORY TO ALL BRANCHES**
Module 1:
Meaning, Objectives and Characteristics of research, Research methods vs Methodology. Types of research, Descriptive vs Analytical, Applied V/s. Fundamental, Quantitative vs. Qualitative, Conceptual vs. Empirical, Research process, Criteria of good research, Developing a research plan.

Module 2:
Defining the research problem, selecting the problem, Necessity of defining the problem, Techniques involved in defining the problem. Importance of literature review in defining a problem, Survey of literature, Primary and secondary sources, Reviews, Treatise, monographs, patents. Web as a source, searching the web, Identifying gap areas from literature review. Development of working hypothesis.

Module 3:

Module 4:
Aim is to strengthen student’s minds towards high quality research through publications, patents and also to learn research ethics. Publications (8-9 hours).
Research concepts (2 hour), Research importance on economy, Research in India and abroad, Importance of publications, Why, where, when to publish?
Publication ethics (2 hour), Plagiarism (how to use turn it in effectively), International ethics on research, what not to publish, Ethical guidelines, Case studies.
Quality vs quantity (2 hour), Searching literature with high quality, Impact factor, Citations (google scholar vs web of science), H-index, Case studies.
How to write paper (2 hour), In High quality journals, Conference Articles, Poster preparation, PhD thesis, Inclusion of References.
Journal reviewing process(1 hour), Selection of the good journal, Knowledge bout journal template, Refereeing process, Research topic selection, Research today and tomorrow, Lab scale to Industry, Traditional research to Technology based research.
Module 5: Self study
Interpretation and report writing, Techniques of interpretation, Structure and components of Scientific reports, Different steps in the preparation, Layout, structure and language of the Report, Illustrations and tables, Types of report, Technical reports and thesis,

References:
II SEMESTER
Program Core Course Syllabus

II SEMESTER
Program Core Course Syllabus
Mixed Signal Circuit Design

<table>
<thead>
<tr>
<th>COURSE CODE</th>
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<th>COURSE TITLE</th>
<th>Mixed Signal Circuit Design</th>
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**CO-1**
Apply the knowledge of Network theory, Electronic circuit design, VLSI design to obtain **optimised Mixed signal circuits**

**CO-2**
Analyze, Mixed Signal building blocks.

**CO-3**
Design, Data converters for the given specification.

**CO-4**
Ability to **conduct experiments to demonstrate** Mixed Signal building blocks (AMS flow using Cadence), perform research to identify best possible circuit suitable for **Mixed signal operation**

**CO-5**
Ability to make an **effective oral presentation and perform in a team** to build Mixed signal circuits using modern tools.

**Switched capacitor circuits**, Design of sample and hold circuits and comparators.

**Oscillators and Phase Locked Loops**: VCO, Mathematical Model of VCO, PLL, Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

**Data converter fundamentals**


**Reference Book**:

**Lab Experiments**:
1. Design a PLL and measure all the parameters.
2. Design a simple ADC/DAC and measure the data conversion time.
3. To measure INL and DNL of ADC/DAC

**Design for Testability**
<table>
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<th>COURSE TITLE</th>
<th>Design for Testability</th>
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<tr>
<td>CO</td>
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<tr>
<td>CO1</td>
<td>Apply the concept of faults and failure models to generate the number of fault models &amp; Automatic Test Pattern Generator (ATPG) for the given design under test (DUT)</td>
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<tr>
<td>CO2</td>
<td>Analyze and identify the given fault in given CUT(can be logic circuit or memory) and conclude the solution to test these faults</td>
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<tr>
<td>CO3</td>
<td>Ability to generate the Automatic Test Pattern Generator (ATPG) with different techniques using CAD tool.</td>
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<tr>
<td>CO4</td>
<td>Ability to search the research papers and attempt to suggest new solution as a team</td>
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</table>

**Introduction to Testing**


**Logic and Fault Simulation**


**Testability Measures**

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

**Built-In Self-Test**

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

**Boundary Scan Standard**

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

**Power issues in IC Testing**

**Text books:**


**Reference books:**


Real Time Operating Systems

<table>
<thead>
<tr>
<th>COURSE CODE</th>
<th>16ECVEGCRO/16ECELGCES</th>
<th>COURSE TITLE</th>
<th>Real Time Operating Systems</th>
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<td>L-T-P-S</td>
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</table>

CO1: Define, understand and explain concepts of Real Time Operating Systems.

CO2: Apply the knowledge of RTOS in Process & File Management, Inter-process Communication, etc and obtain performance difference when compared to normal OS.

CO3: Analyze the real-time deterministic response from interrupt service routines, signals and real time timers.

CO4: Design high performance software applications with real time deterministic response.

CO5: Develop C programs, execute & demonstrate concepts.

CO6: Ability to make an effective oral presentation on topics allocated by instructor pertaining to RTOS and related high performance computing concepts and Ability to perform in a team to code, compile and execute modular software applications.

Real Time Operating Systems


Objects, Services and I/O

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

Exceptions, Interrupts and Timers

Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

Case Studies of RTOS

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

Text books:

**Reference books:**

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

**Lab Experiments:**

1. Write a C program to copy contents from file1 to file2 by using.
   a. Linux System Calls.
   b. C Library Functions

   Note: the output must be in the following format `cp sourcefile destinationfile`

2. Write a C program to print the following file attributes of a given file.
   a. Number of Hard Links
   b. Inode Number
   c. Size of a file
   d. Group id and User id
   e. Time Stamp Information such as last access, last modified, last change
   f. I/O Block size
   g. File Type

3. Write a C Program
   a. To print the System Resource limit(at least 5) of a process by using getrlimit System call
   b. To modify any two System Resource limit by using setrlimit system call.

4. Write a C Program to catch the following signals
   a. SIGINT
   b. SIGSEGV
   c. SIGFPE
   d. SIGALRM (using alarm system call)
   e. SIGALRM (using setitimer system call)

5. Write a C program to ignore a SIGQUIT signal then reset the default action of the SIGINT signal by using
   a. signal system call
   b. sigaction system call

6. Write a C program to achieve inter process communication mechanism by using
   a. Pipe system call
   b. fifo/named pipe (write two programs, one for sender and another for receiver)

7. Write a C program to
   a. Create a message queue, by taking key value from the command prompt
   b. To send a message to message queue by taking message and key value from the command prompt
   c. To receive a message from a queue, by taking key value and message id from the command prompt

8. Write a C program to protect the critical section of a code by creating a binary semaphore
9. Write
   a. A C Program to store message in a shared memory segment by taking key and message from the command prompt
   b. A C program to demonstrate that more than one process can access the message stored in the shared memory
10. Configure the Linux kernel source code, build and boot the system with the newly built kernel.
## System Verilog and Verification

<table>
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<th>COIDTS</th>
<th>CREIDTS</th>
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<th>SYSTEM VERILOG AND VERIFICATION</th>
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### Course Outcomes

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<tr>
<th>CO-NO</th>
<th>Course Outcomes</th>
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<tbody>
<tr>
<td>CO-1</td>
<td>Define, Understand and Explain OOPs concepts and system Verilog data types</td>
</tr>
<tr>
<td>CO-2</td>
<td>Apply system Verilog constructs to create verification environment</td>
</tr>
<tr>
<td>CO-3</td>
<td>Analyze coverage driven verification for given design under test(DUT)</td>
</tr>
<tr>
<td>CO-4</td>
<td>Design solutions to obtain 100% code coverage and functional coverage by determining the set of input constraints and assertions in test benches.</td>
</tr>
<tr>
<td>CO-5</td>
<td>Simulate the layered test bench architecture using system Verilog and analyze coverage reports</td>
</tr>
</tbody>
</table>

### Verification Concepts:
- Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.

### System Verilog:
- System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.
- SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism.

### Randomization:

### System Verilog:
- Assertions, Introduction to Assertion based verification, Immediate and concurrent assertions.

### Coverage driven verification:
- Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

### Building Test bench:
- Layered testbench architecture.

Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface

### References:
1. Janick Bergeron, Writing Testbenches Using SystemVerilog
2. Chris Spear, SystemVerilog for Verification
3. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, Verification
Methodology Manual for System Verilog

Physical Design

<table>
<thead>
<tr>
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<th>COURSE TITLE</th>
<th>Physical design</th>
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<th>CO</th>
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<tbody>
<tr>
<td>CO-1</td>
<td>Apply the Knowledge gained on the advanced concepts of modern VLSI system</td>
</tr>
<tr>
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<td>design including standard cells, cell libraries, IPs etc to partition, place</td>
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<tr>
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<td>the given netlist using algorithms.</td>
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<tr>
<td>CO-2</td>
<td>Analyse and Estimate the parameters for physical design of Proper ASIC</td>
</tr>
<tr>
<td>CO-3</td>
<td>Ability to run the netlist in EDA tools to perform Physical design.</td>
</tr>
<tr>
<td>CO-3</td>
<td>Ability to work as a team to understand the research papers on Physical design</td>
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<td>and educate other scholars by seminar presentation</td>
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</tbody>
</table>

Libraries


Partitioning and Floor planning

Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition, Fiduccia & Mattheyses, Technology File, Circuit Description Design Constraints, Design planning, Pad placement, power planning, Macro placement, Clock planning.

Placement

Global Placement, detail placement, clock tree synthesis, power analysis.

Routing (clock, power/ground, signal nets):

Special routing, Global routing, Detailed routing, Extraction

Verification

Functional Verification,
Timing verification (STA),
Physical Verification, SI analysis, Power Analysis

Text Book:

Reference books:


Hardware/Software Co-design

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<tr>
<th>COURSE CODE</th>
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<th>COURSE TITLE</th>
<th>Hardware/Software Co-design</th>
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<tr>
<th>CO</th>
<th>Course Outcomes</th>
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<tbody>
<tr>
<td>CO-1</td>
<td>Understand fundamental issues in co-design</td>
</tr>
<tr>
<td>CO-2</td>
<td>Learn about prototyping and emulation</td>
</tr>
<tr>
<td>CO-3</td>
<td>Understand compilation techniques, and learn related tools</td>
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<td>CO-4</td>
<td>Acquire ability to differentiate various target architectures</td>
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<tr>
<td>CO-5</td>
<td>Acquire ability to generate specifications and develop verification plans</td>
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</table>

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design
verification, implementation verification, verification tools, interface verification

**Languages for System – Level Specification and Design-I:** System – level specification, design representation for system level synthesis, system level specification languages,

**Languages for System – Level Specification and Design-II:** Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

**Text books:**

**Reference books:** 1. A Practical Introduction to Hardware/Software Co-design - Patrick R. Schaumont - 2010 – Springer

**System On Chip Architecture**

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**CO- No | Course Outcomes**
---|---
CO-1 | **Apply** concepts of Moore’s law, CMOS scaling to understand the System on Chip with its need, evolution, challenges, goals, superiority over system on board & stacked ICs in package.
CO-2 | **Analyze** Typical goals in SoC design and also inter connect architecture
CO-3 | **Design** solutions for issues at system level, and issues of Hardware-Software co design


MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design

Case Study: A Low Power Open Multimedia Application Platform for 3G Wireless.

Reference Books:

Embedded design using ARM architecture

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CO1 Acquire the knowledge on ARM organization and the feature rich ARM Cortex architecture and to understand serial communication techniques with microcontroller. apply skills to model complete Embedded System.

CO2 Analyze digital and analog peripherals, memory of ARM Cortex-Mx microcontrollers

CO3 Conduct experiments with ARM Cortex board to develop various application

CO4 Ability to Demonstrate the development of embedded applications using ARM Cortex platforms, in a team or individual


Lab: Introduction to mbed/similar development board, Keil/similar IDE environment, Blinky Code, Key Input Single/linear/matrix, Interfacing character & graphic LCD.

ARM Cortex – M Architecture Programming Model, Instruction Set, Interrupts & Exception Handling, Timers & PWM
Lab: Experiments with Timers, Generation of 3 phase PWM, Sine wave generation, speed control of DC motor using PWM

Memory model, DMA, Floating Point Operations, Serial Communication peripherals: UART+SPI+I2C, Cortex Microcontroller Software Interface Standard

Lab: Interfacing two devices using UART, Read/Write Memory chip using SPI, Interface RTC chip using I2C

Analog peripherals ADC, DAC, interfacing analog sensors like, temperature, pressure sensors. Low power configurations of ARM microcontrollers

Lab: Generating waveforms using DAC, Acquiring analog signals using ADC and characterizing using FFT

DSP on ARM Cortex-M4, Developing Closed Loop & PID Control Systems

Lab: Interfacing with PC using Serial peripherals are using wireless devices

Reference Books:

Memory Design and Testing

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CO1 Acquire the knowledge on Semiconductor memories

CO2 Ability to Apply the knowledge of CMOS technology and electronic circuits theory to design semiconductor memories

CO3 Ability to Analyze different types of memories.

CO4 Model and Design for Reliability and analyse radiation effect

CO5 Ability to submit a report on the impact/growth of Advanced Memory Technologies for societal and sustained development.


Dynamic Random Access Memories (DRAMs): DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS DRAMs, Soft Error Failures in DRAMs, Advanced DRAM Designs and Architecture, Application Specific DRAMs.
**Non-volatile Memories:** Masked Read-Only Memories (ROMs), High Density ROMs, Programmable Read Only Memories (PROMs), Bipolar PROMs, CMOS PROMs, Erasable (UV), Programmable Road-Only Memories (EPROMs), Floating-Gate EPROM Cell, One-Time Programmable (OTP) EPROMS, Electrically Erasable PROMs (EEPROMs), EEPROM Technology and Architecture, Non-volatile SRAM, Flash Memories (EPROMs or EEPROM), Advanced Flash Memory Architecture.


**Advanced Memory Technologies and High-Density Memory Packaging Technologies:** Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs. Analog Memories, Magneto resistive Random Access Memories (MRAMs). Experimental Memory Devices. Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM Testing and Reliability Issues, Memory Cards, High Density Memory Packaging Future Directions.

**Text Books**
2. Luecke Mize Care, “Semiconductor Memory design & application”, Mc-Graw Hill.

**Advanced Computer Architecture**

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CO1: Acquire knowledge on the basic concepts of computer design, identifying the performance parameters and quantitative principles.

CO2: Recognize the instruction level parallelism and different methods used for scheduling and structuring the code.

CO3: Analyse the performance and Identify the limitations of ILP for the efficiency of multi pipeline architecture

CO4: Understand the memory hierarchy, the I/O system and their impacts on system
CO5  Recognize the performance improvements by implementing shared memory and cache coherence and Identify associated issues in Inter-processor communication.

**Introduction and Review of Fundamentals of Computer Design:** Introduction; Classes computers; Defining computer architecture; Trends in Technology; Trends in power in Integrated Circuits; Trends in cost; Dependability, Measuring, reporting and summarizing Performance; Quantitative Principles of computer design.

**Some topics in Pipelining, Instruction** – Level Parallelism, Exploitation and Limits on ILP: Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining; Basic concepts and challenges of ILP.

**Memory Hierarchy Design, Storage Systems:** Review of basic concepts; Crosscutting issues in the design of memory hierarchies; Case study of AMD Opteron memory hierarchy; Fallacies and pitfalls in the design of memory hierarchies.

**Advanced topics in disk storage:** Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls Definition and examples of real faults and failures; I/O performance, reliability measures, and benchmarks, Queuing theory; crosscutting issues.

**Hardware and Software for VLIW and EPIC Introduction:** Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism.


**References:**

Institutional elective
Institutional elective

ADVANCED MICRO & NANO DEVICES

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CO1 | Acquire knowledge on the fundamental concepts of nano science engineering.
CO2 | Analyse properties of different types of nano structure
CO4 | Ability to submit a report on the impact/growth of micro/nano devices on societal and sustained development and also to submit report on fabrication of nano structures
CO5 | Involve in independent/team learning, Communicate effectively and engage in life-long learning


Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nano meter length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nano materials, ordering of nano systems.

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk, surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.


Hetero Structures and Quantum Well devices: Quantization and low-dimensional electron gas, band alignment in Si/SiGe hetero-structures, HEMTs, Carbon Nano-tube, Graphene device.

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nano crystals, colloidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural.

Methods of measuring properties structure: atomic, crystallography, microscopy, spectroscopy. Properties of nanoparticles: metal nano clusters, semiconducting nanoparticles,

**Text Book:**

**Reference Book:**

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<th>COURSE TITLE</th>
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**CO1** Acquire knowledge on the fundamentals in Robotics namely Kinematics, Controls, sensors and actuators

**CO2** Apply the knowledge of signal processing in Vision and Processing and to move towards Higher-Level Vision.

**CO3** Analyse the integration of Kinematics, Sensors and Control system

**CO4** Build prototype robot on his/her own and demonstrate the basic physics and mathematics behind it

**CO5** Involve in independent/team learning, Communicate effectively and engage in lifelong learning

**Introduction:** Objectives, Classification of robots, Major components of robot, definitions: Kinematics, Controls, and actuators. Robot history, types and applications current and future with examples. Fixed and flexible automation


**Control of Actuators:** Objective, Motivation, Closed loop control in position servo, Effect of friction and gravity, Adaptive control, Optimal control, Computed torque technique,
Transfer function of single joint, Position control for single joint, Brief discussion on performance and stability criteria.

**Sensors**  
Robotic system, Sensor definition and classification, Sensor characteristics, Sensor calibration, Range sensing techniques: Triangulation, Structured light approach, Time of flight, Binary sensors, Analog sensors, Position sensors or Displacement sensor - Potentiometers, Encoders, LVDT, Resolvers, Hall Effect sensors. Velocity sensor-Tachometers (Magnetic and optical encoders). Force and Pressure sensors or Force and Torque sensing - Piezoelectric, Strain gauge, Proximity sensors - Magnetic, Optical, Ultrasonic, Inductive, Capacitive, Eddy-current sensors, Touch and tactile sensor, Torque sensors, Elements of a Wrist sensor. SAMs

**Vision and Processing:**  
Image acquisition, illumination Techniques, imaging geometry, some basic transformations, perspective transformations. Camera model, camera calibration, stereo imaging.

**Higher-Level Vision:**  
Segmentation, Edge Linking and Boundary detection, Thresholding, Region-oriented segmentation, Use of motion, Description, Boundary descriptors, Regional descriptors

**TEXT BOOKS:**
2. “Robotic Engineering” - Richard D Klafter, PHI

**REFERENCE BOOKS:**
2. “Mechatronics” - W. Bolton
Master of Technology

In

VLSI Design and Embedded system

III SEMESTER
Course Title: INTERNSHIP

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**COURSE OUTCOMES**

<table>
<thead>
<tr>
<th>CO1</th>
<th>Ability to develop a sound theoretical and practical knowledge of new technologies.</th>
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<tbody>
<tr>
<td>CO2</td>
<td>Ability to Develop domain specific problem solving and critical thinking skills</td>
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<tr>
<td>CO3</td>
<td>Ability to develop individual responsibility towards their internship goal as well as participate as an effective team member</td>
</tr>
<tr>
<td>CO4</td>
<td>To gain exposure to professional work culture &amp; practices</td>
</tr>
<tr>
<td>CO5</td>
<td>Develop effective presentation &amp; communication skills, and create proper documentation of the work</td>
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Course Title: Project work (I-phase)

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<tr>
<th>COURSE OUTCOMES OF I-</th>
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<tbody>
<tr>
<td>CO1</td>
</tr>
<tr>
<td>Identify a suitable project making use of the technical and engineering knowledge gained from previous courses with the awareness of impact of technology on the Society and their ethical responsibilities.</td>
</tr>
<tr>
<td>CO2</td>
</tr>
<tr>
<td>Collect and disseminate information related to the selected project within given time frame.</td>
</tr>
<tr>
<td>CO3</td>
</tr>
<tr>
<td>Communicate technical and general information by means of oral as well as written Presentation skills with professionalism.</td>
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phase
Master of Technology

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VLSI Design and Embedded system

IV SEMESTER
Course Title: PROJECT WORK (FINAL PHASE)

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<tr>
<th>COURSE CODE</th>
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<th>COURSE TITLE</th>
<th>PROJECT WORK (Final-Phase)</th>
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**COURSE OUTCOMES – phase-II**

<table>
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<tr>
<th>CO1</th>
<th>Identify the modern tools required for the implementation of the project.</th>
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<tbody>
<tr>
<td>CO2</td>
<td>Design, examine critically and implement or develop a prototype for the identified problem during Phase I</td>
</tr>
<tr>
<td>CO3</td>
<td>Communicate technical information by means of oral as well as written presentation skills with professionalism and engage in life-long learning.</td>
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Course Title: Technical Seminar

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**COURSE OUTCOMES**

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<thead>
<tr>
<th>CO1</th>
<th>Identify the problem through literature survey by applying depth knowledge of the chosen domain</th>
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<tbody>
<tr>
<td>CO2</td>
<td>Analyse, synthesize and conceptualize the identified problem</td>
</tr>
<tr>
<td>CO3</td>
<td>Communicate clearly, write effective reports and make effective presentations following the professional code of conduct and ethics</td>
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