BMS COLLEGE OF ENGINEERING, BENGALURU-19

Autonomous Institute, Affiliated to VTU

Department of Electronics and Communication Engineering

Scheme and Syllabus: M.Tech (ELECTRONICS)

Batch 2016 onwards

INSTITUTE VISION

Promoting Prosperity of mankind by augmenting human resource capital through Quality Technical Education & Training

INSTITUTE MISSION

Accomplish excellence in the field of Technical Education through Education, Research and Service needs of society

DEPARTMENT VISION

To emerge as a Centre of Academic Excellence in Electronics, Communication and related domains through Knowledge acquisition, knowledge dissemination and Knowledge generation meeting the global needs and standards

DEPARTMENT MISSION

Imparting quality education through state of the art curriculum, conducive learning environment and Research with scope for continuous improvement leading to overall Professional Success

PROGRAM EDUCATIONAL OBJECTIVES

PEO1: Graduates shall be capable of building their career in related industries, R&D establishments as well as in Teaching with their scholarly knowledge with respect to advanced topics in applied electronics and VLSI Engineering.

PEO2: Graduates shall be capable of conceptualizing and analyzing engineering problems of societal importance related to embedded systems, VLSI and signal processing conduct independent Research leading to technology solutions and communicate the outcomes through verbal and written mechanisms

PEO3: Graduates shall be able to collaborate, manage and execute projects in teams using appropriate tools/technologies with utmost professionalism and acceptable good practices

PROGRAM OUTCOMES

Program Outcomes (POs), are attributes acquired by the student at the time of graduation. The POs are aligned to the Graduate Attributes (GAs) specified by National Board of Accreditation (NBA). These attributes are measured at the time of Graduation, and hence computed every year for the outgoing Batch. The POs are addressed and attained through the Course Outcomes (COs) of various courses of the curriculum.

PO1: Ability to acquire scholarly knowledge in Electronics and VLSI engineering along with a thorough knowledge of their applications

PO2: Ability to analyze complex engineering problems critically and make creative advances for conducting research in a broader context of the problem

PO3: Ability to conceptualize and analyze problem space and solution space of engineering problems pertaining to electronics and VLSI engineering and to arrive at feasible solutions with due considerations towards societal and environmental factors, as applicable

PO4: Ability to conduct research in electronics, VLSI and application areas through formal literature survey and experimentation thus contributing to scientific or technological knowledge

PO5: Ability to analyze, select, learn and apply appropriate techniques, resources, and engineering tools in the area of electronics and VLSI engineering

PO6: Ability to collaborate and carry out multidisciplinary work and to demonstrate self-management and team work in a professional manner with result orientation

PO7: Ability to manage projects efficiently with respect to engineering and finance based on sound management practices.

PO8: Ability to communicate complex engineering activities through technical documentation and presentations

PO9: Ability to engage in lifelong learning thus being able to adapt themselves for technological advancements

PO10: Ability to appreciate and follow professional ethics and also to demonstrate the potential towards social responsibility

PO11: Ability to incorporate corrective measures based on previous mistakes without any explicit feedback

Total Number of Credits (I Sem – IVSem) = 100 Credits

Distribution of credits:

Category	**No of Credits**
Programme Core Course	30
Programme Elective Course	14
All programme core Course	02
Institution Elective Course	04
Internship	21
Technical seminar	02
Project Work	27

M.Tech. (ELECTRONICS)

I Semester **CREDIT BASED**

Subject Code	Course Title	Credits				CREDITS
		L	T	P	S	
16ECELGCAM/ 16ECDCGCAM	Advanced Mathematics	3	0	0	0	3
16ECELPCDL	Digital Circuits and Logic Design	3	1	0	0	4
16ECELGCES/ 16ECVEGCES	Advanced Embedded Systems	3	0	1	1	5
16ECELPCDH	Digital System design using HDL	3	0	1	1	5
16ECELPEZZ	Elective -1	3	0	0	0	3
16ECELPEZZ	Elective - 2	3	0	0	0	3
16APRDICRM	Research Methodology	2	0	0	0	2
	Total	**20**	**1**	**2**	**2**	**25**

Note : Two electives to be chosen from the list below:
Elective will be offered for a minimum strength of six candidates (out of 18) / eight candidates (out of 24)

Course Elective			
16ECELPEDV/ 16ECVEPCDV	Digital VLSI Design	16ECELGELP/ 16ECVEGELP	Low Power VLSI Design
16 ECELPEAE	Automotive Electronics	16 ECELPEME	MEMS
16 ECELPESA	Speech and Audio Processing	16 ECELPECR	Cryptography

Pl. Note: The Course Code: 16 (year), EC(Electronics & Communication), EL(Electronics) PC/PE (Programme core)/Programme elective), ZZ(course abbreviation), GC/GE-Group core/Group Elective

AP (all programme), RD(Research & Development), IC(Institution Core)

M.Tech. (ELECTRONICS)

II Semester ` **CREDIT BASED**

Subject Code	Course Title	Credits				CREDITS
		L	T	P	S	
16ECELPCVV	VLSI Design and Verification	3	0	0	1	4
16ECELPCSD	Synthesis & Optimization of Digital Circuits	3	1	0	0	4
16ECELGCRO/ 16ECVEGCRO	Real Time operating system	3	0	1	1	5
16 ECELPEZZ	Elective -3	3	1	0	0	4
16ECELPEZZ	Elective -4	3	1	0	0	4
16ECELIEZZ	Institution Elective	4	0	0	0	4
	Total	**19**	**3**	**1**	**2**	**25**

Note: Two electives to be chosen from the list below:
Elective will be offered for a minimum strength of six candidates (out of 18) / eight candidates (out of 24)

Course Elective			
16 ECELPEDC	Digital signal compression	16 ECELPEIV	Image and Video Processing
16ECELGEAN/ 16ECDCGEAN	Advanced Computer Networks	16ECELGEAD/ 16ECDCGCAD	Advanced DSP
16ECELGEDE/ 16ECDCGEDE	Detection and Estimation Techniques	16ECELGEAC/ 16ECVEGEAC	Advanced Computer Architecture

Institution Elective	
16ECELIESM	Simulation, Modelling and Analysis

Pl. Note: The Course Code: 16 (year), EC (Electronics & Communication), EL (Electronics), PC/PE (Programme core)/Programme elective), ZZ(course abbreviation), GC/GE-Group core/Group Elective.

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III Semester **CREDIT BASED**

Subject Code	Course Title	Credits				CREDITS
		L	T	P	S	
16ECELPCIN	Internship	0	0	21	0	21
16ECELPCP1	Project work (I-phase)	0	0	4	0	4
	Total	**0**	**0**	**25**	**0**	**25**

Pl. Note: The Course Code: 16 (year), EC(Electronics & Communication), EL(Electronics) PC(Programme core)

M.Tech. (ELECTRONICS)

IV Semester **CREDIT BASED**

Subject Code	Course Title	Credits				CREDITS
		L	T	P	S	
16ECELPCP2	Project work (final phases)	0	0	23	0	23
16ECELPCTS	Technical Seminar	0	0	02	0	02
	Total	**0**	**0**	**25**	**0**	**25**

Pl. Note: The Course Code: 16 (year) , EC (Electronics & Communication), EL(Electronics), PC (Programme core).

M. Tech- ELECTRONICS

I SEMESTER

Programme Core Syllabus

COURSE CODE	16ECELGCAM/ 16ECDCGCAM	COURSE TITLE	ADVANCED MATHEMATICS
CREDITS	3	L-T-P-S	3-0-0-0

COURSE OUTCOME

CO1	Ability to thoroughly understand the concepts, types and characterization of random variables and stochastic processes, along with expectation operator	PO1
CO2	Ability to develop an analytical approach for solving real life problems using the theoretical concepts of probability and statistics	PO1
CO3	Ability to model engineering domains and their dynamics, mathematically, using multidimensional space and the associated linear transformations	PO2
CO4	Ability to analyze engineering data amidst fitment and variability using SVD and PCA techniques for data reduction, data interpretation and system identification with real life case studies	PO2
CO5	Ability towards teamwork by working on problem sheets in groups throughout the semester	PO6

Random Variables Discrete and continuous type Random Variables, Distribution and Density Functions: PMF, CDF, PDF, Gaussian random variable, and other standard random variables, Expectation operator, Multiple random variables: Joint PMF, CDF, PDF, Expectation involving multiple Random variables.

Random Processes: Definition and characterization, Stationary and Ergodic Random processes, Autocorrelation function and its properties, Example Processes: introduction to Markov process, Gaussian Process, Poisson Process.

Vector Spaces and subspaces: Vector spaces, null space, independence, basis and dimension, projections, Least squares approximations, orthonormal bases and Gram-Schmidt.

Advanced Matrix Theory: Introduction to Eigen values and eigen vectors, Positive definite matrices, Singular value decomposition, bases and matrices in SVD, Principal component analysis by SVD, geometry of SVD, idea of linear transformation, matrix representation, search for a good basis, example applications.

REFERENCE BOOKS:

1. S L Miller and D C Childers**, "Probability and random processes: application to signal processing and communication**", Academic Press / Elsevier 2004.

2. A. Papoulis and S U Pillai, **"Probability, Random variables and stochastic processes",** McGraw Hill 2002

3. Peyton Z Peebles**, "Probability, Random variables and Random signal principles",** TMH, 4th Edition 2007

4. MIT Open courseware**, Introduction to Linear Algebra, Course 18.06**

COURSE CODE	16ECELPCDL	COURSE TITLE	DIGITAL CIRCUITS AND LOGIC DESIGN
CREDITS	4	L-T-P-S	3-1-0-0

COURSE OUTCOMES

CO1	Acquire knowledge to analyse threshold gates and their synthesis	PO1
CO2	Able to define, characterize and classify various fault tolerance and apply diagnosis technique to complex systems.	PO3
CO3	Able to learn and design synchronous sequential circuits	PO3
CO4	Will have the capability to identify the various state identification and fault detection experiments	PO1

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks.

Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design.

Capabilities, Minimization, and Transformation of Sequential Machines: The Finite-State Model, Further Definitions, Capabilities and Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of incompletely specified machines.

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks.

State—Identifications and Fault-Detection Experiments: Homing Experiments, Distinguishing Experiments, Machine Identification, and Fault-Detection Experiment.

REFERENCE BOOKS:

1. ZviKohavi, “Switching and Finite Automata Theory”, 2nd Edition. Tata McGraw Hill

2. Charles Roth Jr., “Digital Circuits and logic Design”,Jaico publishing house, 2003.

3. Parag K Lala, “Fault Tolerant and Fault Testable Hardware Design”, Prentice Hall Inc.1985

COURSE CODE	16ECELGCES/ 16ECVEGCES	COURSE TITLE	ADVANCED EMBEDDED SYSTEMS
CREDITS	5	L-T-P-S	3-0-1-1

COURSE OUTCOMES

CO1	Understand and explain the concepts of Embedded Systems and Apply the knowledge of Computer Architecture in building Embedded Systems.	PO1,PO3
CO2	Analyze the real-time deterministic response of embedded systems and various peripherals involved in Embedded system	PO2
CO3	Design low power, real time deterministic Embedded Systems and Develop C programs, execute & demonstrate on embedded target boards like Beagle Bone Black, Raspberry Pi, Arduino, etc.	PO2,PO3, PO5
CO4	Perform in a team to design and develop useful embedded systems and Make an effective oral presentation on topics allocated by instructor pertaining to Computer Architecture, Embedded Systems, Analog and Digital peripherals.	PO9,PO7, PO6,PO8

Introduction to Embedded Systems, Real time nature of ES, Architectures of ES including multi core architecture, Graphic Processing Units(GPU), Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components. Case Study Raspberry Pi 3.

Characteristics and Quality Attributes of Embedded Systems: Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software Trade-offs. Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages(C, C++, Python, VHDL/Verilog).

Introduction to SoC: Case Study Xilinx Zynq, Anatomy, Design Reuse, Abstraction, SoC Design Flow, Zynq APU, ARM Model, Logic Fabric, Block RAM, GPIO, Communication Interfaces, ZynqSoc Design Overview.

Device Comparison: Device Selection Criteria, Zynqvs FPGA, Zynqvs Standard Processor, ZynqvsDicrete FPGA Processor, Zynq Architecture and Design Flow, Embedded Systems and FPGA, Processors and Buses.

USB Basics: Uses and limits, Benefits, Evolution, Bus components, Division of labor, Transfer basics, Elements of a transfer, USB 2.0 transactions, Ensuring successful transfers, Control transfers, Bulk transfers, Interrupt transfers, Isochronous transfers, Enumeration: Process and Descriptors.

Hosts for Embedded Systems: Targeted Host, Targeted Peripheral List, Targeted Host types, Bus current, turning off bus power, Embedded Hosts, Differences from conventional host ports, Functioning as a USB device, OTG devices, A-Device and B-Device, OTG descriptor, Host Negotiation Protocol, Role Swap Protocol

REFERENCES:

1. Hennessy and Patterson, Computer Architecture: A Quantitative Approach", Latest Edition
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009
3. The Zynq Book, by Crockett, Elliot, Enderwitz& Stewart, University of Strathclyde Glasgow, 2014
4. USB Complete: The Developer's Guide, Jan Axelson

Lab Experiments:

1. **Raspberry Pi 3**: Booting the Board with multiple OS, Programming of GPIO, Programming of Serial Peripherals, Control of ADC.
2. **Zynq Board**: Implement Timers and GPIO modules in FPGA and control it with ARM SOC.
3. **Implement a USB generic serial emulator device** on FPGA; interface it with Raspberry Pi 3.

COURSE CODE	16ECELPCDH	COURSE TITLE	DIGITAL SYSTEM DESIGN USING HDL
CREDITS	5	L-T-P-S	3-0-1-1

COURSE OUTCOMES

CO1	Apply the knowledge of constructs and conventions of Verilog / System Verilog for digital system design.	PO1
CO2	Analyse different combinational and sequential digital systems and its design methodology	PO2
CO3	Design combinational and sequential digital systems using Verilog / System Verilog	PO3
CO4	Conduct experiments to demonstrate concepts related to HDL using Verilog/System Verilog	PO5
CO5	Work in teams to design and demonstrate an application of digital system using Verilog and make an effective oral presentation and documentation.	PO5,PO6, PO8

Introduction and Methodology: Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology**.**

Combinational Basics: Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits**,** Verilog modeling of combinationalCircuits.

Sequential Basics: Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology, Verilog modeling of sequential Circuits.

Memories: Concepts, Memory Types, Error Detection and Correction**.**

System Verilog: Overview of System Verilog, Building blocks - Modules, programs, subroutines, package, interface with example code

Language Constructs: Data Types and Operators, Loops and Flow control, System Verilog Tasks and Functions, SV Arrays and Queues.

REFERENCES:

1. Peter J. Ashenden, **"Digital Design: An Embedded Systems Approach Using VERILOG"**, Elesvier, 2010.

2. Stuart S, Simon D& Peter "**System Verilog for Design"** Springer publication

3. Ben Cohen, Srinivasan V, Ajeetha Kumari& Lisa Kumari "**System Verilog Assertions Handbook"**, 3rd Edition for Dynamic and Formal Verification,2013.

4. Chris Spear, "**SystemVerilog for Verification"**

5. http://www.testbench.in

Lab Experiments:

1. Write Verilog code for the design of 8-bit
i. Carry Look Ahead adder
ii. Ripple Carry Adder
iii .BCD Adder & Subtractor

2. Write a Verilog code for the design of 8-bit Booth's multiplier

3. Write a Verilog code to design a 8-bit Magnitude comparator

4. Write a Verilog code to design a 4-bit universal shift register

5. Write a Verilog code to design 8-bit parity generator

6. Write Verilog Code for 3-bit Arbitrary Counter to generate 0,1,2,3,6,5,7 and repeats.

7. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.
Eg 11101 (with and without overlap) etc.,

COURSE CODE	16APRDICRM	COURSE TITLE	RESEARCH METHODOLOGY
CREDITS	2	L-T-P-S	2-0-0-0

Module 1:
Meaning, Objectives and Characteristics of research, Research methods Vs. Methodology, Types of research, Descriptive Vs. Analytical, Applied Vs. Fundamental, Quantitative Vs. Qualitative, Conceptual Vs. Empirical Research process, Criteria of good research, Developing a research plan.

Module 2:
Defining the research problem, selecting the problem, Necessity of defining the problem, Techniques involved in defining the problem ,Importance of literature review in defining a Problem, Survey of literature, Primary and secondary sources , Reviews, treatise, monographs patents, web as a source, searching the web, Identifying gap areas from literature review, Development of working hypothesis.

Module 3:
IPRs, Invention and Creativity, Intellectual Property, Importance and Protection of Intellectual Property Rights (IPRs), a brief summary of Patents, Copyrights, Trademarks, Industrial Designs, Integrated Circuits, Geographical Indications, Establishment of WIPO ,Application and Procedures.

Module 4:
Aim of this part of the course: is to strengthen student's minds towards high quality research through publications, patents and also to learn research ethics. Publications (8-9 hours)

Research concepts (2 hour) Research importance on economy, Research in India and abroad, Importance of publications, Why, where, when to publish?

Publication ethics (2 hour), Plagiarism (how to use turn it in effectively), International ethics on research, what and what not to publish, Ethical guidelines, Case studies

Quality vs quantity (2 hour) Searching literature with high quality, Impact factor, Citations (Google scholar vs. web of science), H-index, Case studies

How to write paper (2 hour), In High quality journals, Conference Articles, Poster preparation, PhD thesis, Inclusion of References

Journal reviewing process (1 hour), Selection of the good journal, Knowledge bout journal template, Refereeing process, Research topic selection, Research today and tomorrow, Lab scale to Industry, Traditional research to Technology based research.

Module 5: Self study
Interpretation and report writing, Techniques of interpretation, Structure and components of Scientific reports, Different steps in the preparation , Layout, structure and language of the Report, Illustrations and tables , Types of report, Technical reports and thesis.

REFERENCES:

1. Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., 2002. An introduction to Research Methodology, RBSA Publishers.
2. Kothari, C.R., 1990. Research Methodology: Methods and Techniques. New Age International. 418p.
3. Anderson, T. W., An Introduction to Multivariate Statistical Analysis, Wiley Eastern Pvt., Ltd., New Delhi
4. Sinha, S.C. and Dhiman, A.K., 2002. Research Methodology, EssEss Publications. 2 volumes.
5. Trochim, W.M.K., 2005. Research Methods: the concise knowledge base, Atomic Dog Publishing. 270p.
6. Day, R.A., 1992.How to Write and Publish a Scientific Paper, Cambridge University Press.
7. Fink, A., 2009. Conducting Research Literature Reviews: From the Internet to Paper. Sage Publications
8. Coley, S.M. and Scheinberg, C. A., 1990, "Proposal Writing", Sage Publications.
9. Intellectual Property Rights in the Global Economy: Keith Eugene Maskus, Institute for International Economics, Washington, DC, 2000
10. Subbarau NR-Handbook on Intellectual Property Law and Practice-S Viswanathan Printers and Publishing Private Limited.1998

M. Tech- ELECTRONICS

I SEMESTER

Programme Elective Syllabus

COURSE CODE	16ECELGEDV/ 16ECVEGCDV	COURSE TITLE	DIGITAL VLSI DESIGN
CREDITS	3	L-T-P-S	3-0-0-0

COURSE OUTCOMES

CO1	Apply the concepts of MOS system in digital VLSI design	PO1
CO2	Analyse the electrical and physical properties, Switching characteristics and interconnect effect of a MOS system in digital VLSI design	PO2
CO3	Design dynamic logic circuits, Semiconductors Memory circuits, and different CMOS logic circuits.	PO3
CO4	Use modern tools to simulate Schematic and Layout of Digital circuits individually/ in group (s) and Make an effective oral presentation and documentation on advanced topics related to the course by referring IEEE Journals.	PO5,PO6, PO8

MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.

MOS Inverters: Static Characteristics of CMOS Inverter. MOS Inverters, Layout and stick diagrams

Switching Characteristics and Interconnect Effects: Delay-Time Definition, Calculation, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitic, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM).

REFERENCES:

1. Sung Mo Kang &YosufL eblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.

2. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.

COURSE CODE	16ECELPEAE	COURSE TITLE	AUTOMOTIVE ELECTRONICS
CREDITS	3	L-T-P-S	3-0-0-0

COURSE OUTCOMES

CO1	Ability to carry out quantitative and qualitative assessment of performance of automotives in terms of the underlying system dynamics with emphasis on emission and fuel consumption	PO1,PO2
CO2	Ability to design and implement in-vehicle communication systems of varied capabilities and capacities as electronic embedded systems	PO3
CO3	Ability to architect (for new development) or migrate (in case of existing design) automotive ECUs and infrastructure requirements in compliance to state-of-the-art standards	PO2,PO3

Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System, Battery, Starting System

Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition Control, Idle sped control, EGR Control

Air/Fuel Systems – Fuel Handling, Air Intake System, Air/ Fuel Management

Exhaust After-Treatment Systems – AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems

Vehicle Motion Control – Cruise Control, Chassis, Power Brakes, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension

Integrated Body – Climate Control Systems, Electronic HVAC Systems, Safety Systems – SIR, Interior Safety, Lighting, Entertainment Systems

Automotive Diagnostics – Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics

Sensors and actuators – Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor - Strain gauge and Capacitor capsule, Engine Coolant Temperature (ECT) Sensor, Intake Air

Temperature (IAT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor – Fuel Metering Actuator, Fuel Injector, Ignition Actuator

Automotive in-Vehicle communication systems: Characteristics and constraints, In-car embedded networks: CAN, FlexCAN, TTCAN, Flexray, LIN, MOST and IDB1394 protocols, Car-to-Car (C2C) and Car-to-infrastructure (C2I) communications –Programmers model of communication controllers – communication hardware and bus – case studies

Standardization in Automotive ECU Development: Traditional approach and its shortcomings, Worldwide standards, AUTOSAR based automotive ECU development, AUTOSAR architecture, AUTOSAR methodology, AUTOSAR in practice, Conformance testing, Migration to AUTOSAR, AUTOSAR in OEM-supplier collaboration

Working definition of ITS - Broad scope - Current status of ITS and State-of-the-Art - Fundamental issues in ITS - Principal characteristics of ITS - Scientific validation of ITS designs through modeling and simulation

Modeling and simulation techniques for ITS design - Introduction - Virtual and physical process migration strategies for ITS designs - Software techniques underlying the process migration strategies - Implementation issues - Simulation results and performance analysis

Future issues in ITS - New Meta-level Principles for an untapped ITS technological mine - Examples of formidable challenges and opportunities

REFERENCES:

1.William B. Ribbens, “Understanding Automotive Electronics”, 6th Edition, SAMS/Elsevier Publishing

2.NicolasNavet, “Automotive Embedded Systems Handbook”, Industrial Information Technology Series, CRC press.

3. Robert Bosch GmbH, “Automotive Electrics Automotive Electronics”, 5th edition, Wiley publications.

4. Ronald K Jurgen, “Automotive Electronics Handbook”, McGraw-Hill, Inc, 2nd edition.

5.SumitGhosh, Tony S Lee, “Intelligent Transportation System” – Smart and Green Infrastructure, 2nd Edition CRC Press

COURSE CODE	16ECELPESA	COURSE TITLE	SPEECH AND AUDIO PROCESSING
CREDITS	3	L-T-P-S	3-0-0-0

COURSE OUTCOMES

CO1	Manipulate, and visualize speech and Audio signals – Perform various decompositions, codifications, and modifications.	PO1
CO2	Analyze speech signal to extract the characteristic of vocal tract (formants) and vocal cords (pitch).	PO2
CO3	Design and implement algorithms for processing speech and audio signals considering the properties of acoustic signals and human hearing	PO3
CO4	Ability to make an effective oral presentation and documentation on advanced topics related to the course by referring IEEE Journals.	PO6,PO8

Digital Models for the Speech Signal: Process of speech production, Acoustic theory of speech production, Lossless tube models, and Digital models for speech signals.

Time Domain Models for Speech Processing: Time dependent processing of speech, Short time energy and average magnitude, Short time average zero crossing rate, Speech vs silence discrimination using energy & zero crossings, Pitch period estimation, Short time autocorrelation function, Short time average magnitude difference function, Pitch period estimation using autocorrelation function, Median smoothing.

Digital Representations of the Speech Waveform: Sampling speech signals, Instantaneous quantization, Adaptive quantization, Differential quantization, Delta Modulation, Differential PCM, Comparison of systems, direct digital code conversion

.

Short time Fourier analysis: Linear Filtering interpretation, Filter bank summation method, Overlap addition method, Design of digital filter banks, Implementation using FFT, Spectrographic displays, Pitch detection, Analysis by synthesis, Analysis synthesis systems

Homomorphic Speech Processing: Homomorphic systems for convolution, Complex cepstrum, Pitch detection, Formant estimation, Homomorphic vocoder.

Linear Predictive Coding Of Speech: Basic principles of linear predictive analysis, Solution of LPC equations, Prediction error signal, Frequency domain interpretation, Relation between the various speech parameters, Synthesis of speech from linear predictive parameters.

REFERENCES:

1. L. R. Rabiner and R. W. Schafer**,** "**Digital Processing of Speech Signals**", Pearson Education (Asia) Pte.Ltd., 2004.

2. D. O"Shaughnessy, "**Speech Communications: Human and Machine**", Universities Press, 2001.

3. L. R. Rabiner and B. Juang, "**Fundamentals of Speech Recognition**", Pearson Education (Asia) Pte.Ltd., 2004.

4. Z. Li and M.S. Drew**,** "**Fundamentals of Multimedia"**, Pearson Education (Asia) Pte. Ltd., 2004

COURSE CODE	16ECELGELP/ 16ECVEGELP	COURSE TITLE	LOW POWER VLSI
CREDITS	3	L-T-P-S	3-0-0-0

COURSE OUTCOMES

CO1	Extend the knowledge on basics of MOSFETs and Power Dissipation in MOS circuits to obtain the concepts of different techniques for power optimization.	PO1
CO2	Ability to apply the low power concepts to find the static and dynamic power consumption in a design	PO2
CO3	Ability to design the power optimised circuit for the given specification.	PO2, PO3
CO4	Usage of EDA tool to implement the designed circuit with techniques of power optimisation in the design and justify obtained report by class room presentation.	PO5, PO8
CO5	Understand the journal research papers related to low power and update the knowledge for new techniques to incorporate in projects of the specified stream.	PO9

Basics of MOS circuits, Sources of Power dissipation: Dynamic Power Dissipation -Short Circuit Power, Switching Power, Glitching Power, Static Power Dissipation, Degrees of Freedom.

Supply Voltage Scaling Approaches: Device feature size scaling Multi-Vdd Circuits Architectural level approaches: Parallelism, Pipelining Voltage scaling using high-level transformations Dynamic voltage scaling Power Management

Switched Capacitance Minimization Approaches: Hardware Software Tradeoff Bus Encoding Two's complements Vs Sign Magnitude Architectural optimization Clock Gating Logic styles

Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach Multi-threshold-voltage CMOS (MTCMOS) approach Power gating Transistor stacking Dual-V_t assignment approach (DTCMOS)

Special Topics: Adiabatic Switching Circuits Battery-aware Synthesis Variation tolerant design CAD tools for low power synthesis

Text Books:

1. Sung Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata Mcgrag Hill.

2. A. Bellamour, and M. I. Elmasri, Low Power VLSI CMOS Circuit Design, Kluwer Academic Press, 1995.

3. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995.

REFERENCES:

1.Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Inter science, 2000.

2.NPTEL http://nptel.iitm.ac.in Computer Science and Engineering, Department of Computer Science and Engineering ,IIT Kharagpur

COURSE CODE	16ECELPEME	COURSE TITLE	MEMS
CREDITS	3	L-T-P-S	3-0-0-0

COURSE OUTCOMES

CO1	Gain a fundamental understanding of standard micro fabrication techniques and the issues surrounding them	PO1
CO2	Critically analyse microsystems technology for technical feasibility as well as practicality.	PO2
CO3	Apply knowledge of micro fabrication techniques and applications to the design and manufacturing of an MEMS device or a microsystem	PO3
CO4	Understand the unique requirements, environments, and applications of MEMS	PO1

Overview of MEMS and Microsystems: MEMs and Microsystems, Evolution of micro fabrication, Microsystems and miniaturization, Application of Microsystems, Markets for Microsystems

Working Principles of Microsystems: Introduction, MEMS and Micro actuators, Microfluidics, Micro actuators with Mechanical inertia.

Engineering Science For Microsystems Design: Introduction, Molecular theory of matter and intermolecular forces, Doping of semiconductor, Plasma physics, Electrochemistry

Thermo fluid Engineering and Microsystems Design: Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization

Designing Arithmetic Building Blocks: Introduction, Basic equation in continuum fluid dynamics, laminar fluid flow in circular conduits, Computational fluid dynamics and incompressible fluid flow in micro-conduits

Microsystems Fabrication Processes: Introduction, Photolithography, Diffusion, Oxidation, Chemical vapour deposition.

REFERENCES:

1. Tai-Ran Hsu, MEMS and Microsystems, 2nd Edition, Wiley, 2008

2. Mohamad Gad El Hak, MEMS Design and Fabrication, 2nd Edition, CRC Press, 2006.

COURSE CODE	16ECELPECR	COURSE TITLE	CRYPTOGRAPHY
CREDITS	3	L-T-P-S	3-0-0--0

COURSE OUTCOMES

CO1	Understand the basic concepts of cryptography and encrypt various types of cipher	PO1
CO2	Learn various encryption standards and Design the various key distribution and management schemes	PO3
CO3	Analyse existing authentication protocols for two party communication and digital signatures	PO2
CO4	Become proficient in the application of Number theory for design of various crypto algorithms.	PO1
CO5	Ability to make an effective oral presentation and explore new ideas in a team	PO4,PO8

Overview: Introduction, Security Trends, The OSI Security Architecture, Security Attacks, Security Services, Security Mechanisms, A Model for Network Security. Classical Encryption Techniques, Symmetric Cipher Model, Substitution Techniques, Transposition Techniques, Rotor Machines, Steganography.

Block Ciphers and the Data Encryption Standard :Block Cipher Principles, The Data Encryption Standard ,The Strength of DES , Differential and Linear Cryptanalysis, Block Cipher Design Principles, Multiple Encryption and Triple DES ,Block Cipher Modes of Operation, Advanced Encryption Standard ,Evaluation Criteria For AES ,The AES Cipher

Public Key Cryptography and Key Management: Principles of Public-Key Cryptosystems, The RSA Algorithm, Key Management, Diffie-Hellman Key Exchange.

Message Authentication and Digital Signature: Message integrity, Random Oracle Model, Message Authentication codes, Digital Signature Process, Services, and Attacks on Digital Signature, Digital Signature Schemes and Applications.

Mathematics of Cryptography: Introduction to Number Theory, Prime Numbers, Fermat's and Euler's Theorems, the Chinese Remainder Theorem, Discrete Logarithms

REFERENCES:

1. William Stallings, **"Cryptography and Network Security"**, 4th Edition, Pearson Education PHI

2. Behrouz A Forouzan, Debdeeep Mukhopadhyay, "**Cryptography and Network Security",** 2nd Edition, McGraw Hill

3. Atul Kahate ," **Cryptography and Network Security",** 2nd edition , Tata McGraw-Hill Publishing Company Limited.

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II SEMESTER

Programme Core Syllabus

COURSE CODE	16ECELPCVV	COURSE TITLE	VLSI DESIGN AND VERIFICATION
CREDITS	4	L-T-P-S	3-0-0-1

COURSE OUTCOMES

CO1	Ability to acquire knowledge on verification and apply for VLSI designs	PO1
CO2	Analyse on verification methodologies and different types of simulators	PO2
CO3	Design a solution to obtain 100% code coverage & functional coverage by determining the set of input constraints and assertions in test benches.	PO3
CO4	Simulate the test bench architecture using system Verilog and analyse coverage reports	PO5
CO5	Ability to work in team for verification of different digital system using EDA tool and make an effective oral presentation	PO5,PO6, PO8

Importance of Verification: Concepts of verification, importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification.

Functional verification approaches: Black box verification, white box verification, grey box verification. Testing versus verification: scan based testing, design for verification. Verification reuse.The cost of verification.

Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modellers, waveform viewers.

Code & Functional Coverage: statement coverage, path coverage, expression coverage, FSM coverage, what does 100%coverage mean? Item Coverage, cross coverage, Transition coverage, what does 100% functional mean? Assertions, Issue tracking & Metrics.

The verification plan: The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies .Directed and random based approach, Directed test cases.

Formal Verification: SAT BDDs, Symbolic Model Checking with BDDs, Model Checking using SAT, Equivalence Checking.

Verification Methodology: Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros.

REFERENCES:

1. Janick Bergeron, **"Writing test benches: functional verification of HDL models"**, 2nd edition ,Kluwer Academic Publishers.

2. https://en.wikipedia.org/wiki/**Universal_Verification_Methodology.**

3**.** The **Verification Methodology Cookbook -** online textbook

4. For Formal Verification - "**Formal Verification -** An Essential Toolkit for Modern VLSI Design"

COURSE CODE	16ECELPCSD	COURSETITLE	SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS
CREDITS	4	L-T-P-S	3-1-0-0

COURSE OUTCOMES

CO1	Understand the process of synthesis and optimization in a top down approach for digital circuits models using HDLs.	PO1
CO2	Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models	PO2
CO3	Apply different two level optimization algorithms for combinational circuits	PO2
CO4	Ability to execute projects after getting familiar with VHDL and Cadence	PO5

Circuits And Models: Design of Microelectronic Circuits - Computer Aided Synthesis and optimization, Boolean algebra and Application,

Hardware Modelling Hardware Modelling Languages, abstract models, compilation and behavioural optimization.

Architectural Level Synthesis And Optimization: The Fundamental Architectural synthesis Problems-Area and performance Estimation- Critical path, Control unit synthesis-synthesis of pipelined circuits.

Scheduling Algorithms and Resource Sharing: model for the scheduling problems, Unconstrained Scheduling-ASAP Algorithm-ALAP Scheduling Algorithm- Scheduling with Resource Constraints.

Logic-Level Synthesis and Optimization: Logic optimization Principles, operations on two level logic covers, Algorithms and logic Minimization and Encoding problems-

REFERENCES:

1. Giovanni De Micheli, “Synthesis and optimization of Digital Circuits”, Tata McGraw-Hill, 2003.

2. John Paul Shen, Mikko H. Lipasti, “Modern processor Design”, Tata McGraw Hill, 2003

COURSE CODE	16ECELGCRO/ 16ECVEGCRO	COURSE TITLE	REAL TIME OPERATING SYSTEMS
CREDITS	5	L-T-P-S	3-0-1-1

COURSE OUTCOMES

CO1	Define, understand and explain concepts of Real Time Operating Systems	PO1
CO2	Apply the knowledge of RTOS in Process & File Management, Inter-process Communication, etc and obtain performance difference when compared to normal OS.	PO3
CO3	Analyze the real-time deterministic response from interrupt service routines, signals and real time timers.	PO2
CO4	Design high performance software applications with real time deterministic response.	PO2,PO3
CO5	Develop C programs, execute & demonstrate concepts.	PO2,PO3, PO5
CO6	Ability to make an effective oral presentation on topics allocated by instructor pertaining to RTOS and related high performance computing concepts and Ability to perform in a team to code, compile and execute modular software applications.	PO6,PO7, PO8,PO9

Introduction: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS,Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization,Communication and Concurrency.Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage,Operations and Use.

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

Text books:

1.Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCES:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.

2. Advanced UNIX Programming, Richard Stevens

3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

Lab Experiments:

1. Write a C program to copy contents from file1 to file2 by using.
    a. Linux System Calls.
    b. C Library Functions

    Note: the output must be in the following format $mycpsource file destination file

2. Write a C program to program to print the following file attributes of given file.
    a. Number of Hard Links
    b. I node Number
    c. Size of a file
    d. Group id and User id
    e. Time Stamp Information such as last access, last modified, last change
    f. I/O Block size
    g. File Type
3. Write a C Program
    a. To print the System Resource limit(at least 5) of a process by using get limit System call
    b. To modify any two System Resource limit by using set limit system call.
4. Write a C Program to catch the following signals
    a. SIGINT
    b. SIGSEGV
    c. SIGFPE
    d. SIGALRM (using alarm system call)
    e. SIGALRM (using set timer system call)
5. Write a C program to ignore a SIGQUIT signal then reset the default action of the SIGINT signal by using
    a. signal system call
    b. sigaction system call
6. Write a C program to achieve inter process communication mechanism by using
    a. Pipe system call
    b. fifo/named pipe (write two programs, one for sender and another for receiver)
7. Write a C program to
    a. Create a message queue, by taking key value from the command prompt
    b. To send a message to message queue by taking message and key value from the command prompt
    c. To receive a message from a queue, by taking key value and message id from the command prompt
8. Write a C program to protect the critical section of a code by creating a binary semaphore
9. Write
    a. A C Program to store message in a shared memory segment by taking key and message from the command prompt

b. A C program to demonstrate that more than one process can access the message stored in the shared memory

10. Configure the Linux kernel source code, build and boot the system with the newly built kernel.

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II SEMESTER

Programme Elective Syllabus

COURSE CODE	16ECELPEDC	COURSE TITLE	DIGITAL SIGNAL COMPRESSION
CREDITS	4	L-T-P-S	3-1-0-0

COURSE OUTCOMES

CO1	Acquire knowledge on coding, quantization ,encoding techniques and apply for signal compression	PO1
CO2	Analyse and evaluate different data compression and coding methods	PO2
CO3	Design a lossless and lossy compression algorithms which can be used for digital signal compression	PO3
CO4	Work in teams towards group assignments and refer IEEE journal papers on advanced compression techniques and give oral presentation	PO4,PO6, PO8

Introduction: Compression techniques, Modelling& coding, Information theory, Models for sources, Coding – uniquely Decodable codes, Prefix codes.

Lossless Coding: Huffman coding, Adaptive Huffman coding, Arithmetic coding, Dictionary techniques – LZ77, LZ78.

Quantization: Quantization problem, Uniform Quantizer, Adaptive Quantization, Non-uniform Quantization, Vector Quantization, LBG algorithm.

Differential Encoding: Basic algorithm, Prediction in DPCM, Adaptive DPCM, Delta Modulation.

Sub-band Coding: Filters, Sub-band coding algorithm, Design of filter banks, Perfect reconstruction using two channel filter banks, M-band QMF filter banks.

Wavelet Based Compression: Wavelets, Image compression – EZW, SPIHT algorithms.

REFERENCES:

1. K. Sayood**,** "**Introduction to Data Compression**," Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.

2. N. Jayant and P. Noll, **"Digital Coding of Waveforms: Principles and Applications to Speech and Video**," Prentice Hall, USA, 1984.

3. D. Salomon, "**Data Compression: The Complete Reference**", Springer, 2000.

COURSE CODE	16ECELGEAN/ 16ECDCGEAN	COURSE TITLE	ADVANCED COMPUTER NETWORKS
CREDITS	4	L-T-P-S	3-1-0-0

CO1	Apply the concepts of Computer Networks and Networks Models for Data Communication.	PO1
CO2	Analyze networking architecture and infrastructure for wired and wireless networks.	PO2
CO3	Apply knowledge of channel condition to various network conditions and hence analyze the network.	PO2
CO4	Ability to identify the future opportunities and challenges associated with next generation networks.	PO4

Introduction: Computer network, Telephone networks, networking principles.

Packet switched networks: Ethernet, Token ring, FDDI, DQDB, frame relay.

Circuit switched Networks: Performance of Circuit switched networks, SONET, DWDM**.**

Internet Protocol: overview of internet protocols, IP, TCP, UDP, performance of TCP/IP networks.

Wireless Networks: Wireless channel, link level design, channel access, network design, Routing protocol requirements, choices, distance vector routing, link state routing, hierarchical routing, multicast routing.

REFERENCES:

1. J. Walrand and P. Varaiya, "High performance communication networks", Harcourt Asia (Morgan Kaufmann), 2000.

2. S. Keshav, "An Engineering approach to Computer Networking", Pearson Education, 1997.

3. A. Leon-Garcia, and I. Widjaja, "Communication network: Fundamental concepts and key architectures", TMH, 2000.

4.J. F. Kurose, and K. W. Ross, "Computer networking: A top down approach featuring the Internet", Pearson Education, 2001

COURSE CODE	16ECELGEDE/ 16ECDCGEDE	COURSE TITLE	DETECTION AND ESTIMATION TECHNIQUES
CREDITS	4	L-T-P-S	3-1-0-0

COURSE OUTCOMES

CO1	Acquire the concepts of detection theory, estimation theory and binary/composite hypothesis testing	PO1
CO2	Apply different techniques to perform detection of deterministic / random signals in the presence of noise	PO1,PO2
CO3	Visualize higher applications of the concept in EC engineering applications through study of relevant IEEE papers	PO9

Hypothesis testing: Binary hypothesis testing, MAP criteria, Bayes' risk, Neyman-Pearson theorem, multiple hypothesis tests, Performance of Binary Receivers in AWGN, Sequential Detection and Performance.

Signal detection with random parameters: Detection of known signals in noise, Matched filter, Performance evaluations, Composite Hypothesis Testing, Unknown Phase, Unknown Amplitude, Unknown Frequency, White and Colored Gaussian Noise for Continuous Signals, Estimator Correlator.

Detection of multiple hypotheses: Bayes Criterion, MAP Criterion, M-ary Detection Using Other Criteria, Signal-Space Representations, Performance of M-ary Detection Systems, Sequential Detection of Multiple Hypotheses, Linear models, Rayleigh fading sinusoid.

Fundamentals of estimation theory: Formulation of the General Parameter Estimation Problem, Relationship between Detection and Estimation Theory, Types of Estimation Problems. Properties of estimators, Applications.

REFERENCES:

1. Harry L. Van Trees,**"Detection, Estimation, and Modulation Theory, Part I,"** John Wiley & Sons, Inc. 2001**.**

2. StevenM.kay**, "Fundamentals of Statistical signal processing, volume-1: Estimation theory".** Prentice Hall 1993**.**

3. A.Papolis and S.UnnikrishnaPillai**, "Probability, Random Variables and stochastic processes",** 4e,.The McGraw-Hill 2002**.**

COURSE CODE	16ECELPEIV	COURSE TITLE	IMAGE AND VIDEO PROCESSING
CREDITS	4	L-T-P-S	3-1-0-0

COURSE OUTCOMES

CO1	Comprehend the basic concepts of image processing and video processing techniques in different domains.	**PO1**
CO2	Apply different transform techniques related to images and video for better visualisation.	**PO1**
CO3	Identify and conceptualise various techniques associated with Image restoration, Image Segmentation, Image Compression and motion estimation for better resolution.	**PO2,PO3**
CO4	Ability to make an effective oral presentation and documentation on advanced topics related to the course by referring IEEE Journals.	**PO8**

Fundamentals of Image Processing: Basic steps of Image Processing System, Sampling and Quantization of an image, relationship between pixels.

Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Image smoothing, Image sharpening, Selective filtering. Image Segmentation, Point, Line and Edge Detection, Thresholding, Region Based segmentation, Image restoration techniques, Image registration.

Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, filtering operations.

2-D Motion Estimation Optical flow: General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

REFRENCES:

1. **Digital Image Processing** – Gonzaleze and Woods, 3rd Ed., Pearson.

2. **Video Processing and Communication** – Yao Wang, JoemOstermann and Ya–quin Zhang. 1st Ed.,PH Int.

3. **Digital Video Processing** – M. Tekalp, Prentice Hall International

4. **Digital Image Processing** – S.Jayaraman, S.Esakkirajan, T.Veera Kumar–TMH, 2009.

COURSE CODE	16ECELGEAD/ 16ECDCGEAD	COURSE TITLE	ADVANCED DSP
CREDITS	4	L-T-P-S	3-1-0-0

COURSE OUTCOMES

CO1	understand the theoretical concepts of advanced DSP, including FIR/IIR filter design, multirate DSP and adaptive filters	PO1
CO2	Visualize and apply the concepts of DSP to real life problems of practical and numerical nature.	PO3
CO3	Work in teams to progress towards group assignments and to choose, read and assimilate one IEEE journal paper covering an application of DSP	PO6, PO2,PO9
CO4	Create a standard documentation and presentation of the work performed by their team	PO8

Introduction: Overview of signals and systems, The concept of frequency in continuous time and discrete time signals, sampling in T/F domain, Analog to digital and digital to analog conversion. Discrete Fourier transform: The DFT / IDFT pair, Properties of DFT, Linear filtering methods based on the DFT. Communication engineering applications.

Design of digital filters: General considerations, design of FIR filters, Design of IIR filters from analog filters.

Multirate digital signal processing: decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Polyphase implementations, Multistage implementation of sampling rate conversion, Engineering applications of multirate signal processing

Adaptive filter: Adaptive direct form FIR filters, The LMS algorithm (without proof), applications of adaptive filters

REFERENCES:

1. Robert. O. Cristi, "**Modern Digital signal processing**", Cengage Publishers, India, 2003.

2. S. K. Mitra, "**Digital signal processing: A computer based approach**", 3rd edition, TMH, India, 2007.

3. E.C. Ifeachor, and B. W. Jarvis,"**Digital signal processing: A Practitioner's approach**", Second Edition, Pearson Education, India, 2002,

4. Proakis, and Manolakis, "**Digital signal processing**", 3rd edition, Prentice Hall, 1996

COURSE CODE	16ECELGEAC/ 16ECDCGEAC	COURSE TITLE	ADVANCED COMPUTER ARCHITECTURE
CREDITS	4	L-T-P-S	3-1-0-0

COURSE OUTCOMES

CO1	Ability to architect high performance computer based on parallel processing paradigms as applicable to "execution unit", "memory subsystem" and "I/O subsystem"	PO1
CO2	Ability to analyze the existing high performance computational infrastructure in terms of their underlying ISA, memory design and I/O design	PO2
CO3	Ability to analyze compiler based techniques which are employed to explore ILP under static conditions	PO2
CO4	Ability to characterize scientific applications and to carry out their performance assessment when deployed on large-scale multiprocessor system with interprocessor communication	PO1,PO2

Introduction and Review of Fundamentals of Computer Design: Introduction; Classes computers; Defining computer architecture; Trends in Technology; Trends in power in Integrated Circuits; Trends in cost; Dependability, Measuring, reporting and summarizing Performance; Quantitative Principles of computer design.

Some topics in Pipelining, Instruction –Level Parallelism, Exploitation and Limits on ILP :Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining; Basic concepts and challenges of ILP.

Memory Hierarchy Design, Storage Systems: Review of basic concepts; Crosscutting issues in the design of memory hierarchies; Case study of AMD Opteron memory hierarchy; Fallacies and pitfalls in the design of memory hierarchies.

Advanced topics in disk storage: Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls Definition and examples of real faults and failures; I/O performance, reliability measures, and benchmarks**,** Queuing theory; crosscutting issues.

Hardware and Software for VLIW and EPIC Introduction: Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism.

Large-Scale Multiprocessors and Scientific Applications Introduction, Interprocessor Communication: The Critical Performance Issue, Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications.

REFERENCES:

1. John L. Hennessey and David A. Patterson, "**Computer Architecture – A quantitative approach",** Morgan Kaufmann / Elsevier, Fifth edition, 2012.

2. Richard Y. Kain, "**Advanced Computer Architecture a Systems Design Approach**", PHI, 2011

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II SEMESTER

Programme Institutional Elective
Syllabus

COURSE CODE	16ECELIESM	COURSE TITLE	SIMULATION,MODELLING AND ANALYSIS
CREDITS	4	L-T-P-S	4-0-0-0

COURSE OUTCOMES

CO1	Ability to understand basics of simulation modeling	PO1
CO2	Ability to apply techniques for increasing validity & credibility	PO1
CO3	Ability to analyze& select different types of probability distributions for output data	PO2
CO4	Ability to design different approaches for Random number generation	PO3

Basic simulation modelling: Nature of simulation, system models, discrete event simulation, single server simulation, alternative approaches, other types of simulation.

Building valid, credible and detailed simulation models: Techniques for increasing model validity and credibility, comparing real world Observations.

Selecting input probability distributions: Useful probability distributions, assessing sample independence, activity I, II and III. Models of arrival process.

Random numbers generators: linear congruential, other kinds, testing random number generators. Random variate generation: approaches, continuous random variates, discrete random variates, correlated random variates.

Output data analysis: Statistical analysis for terminating simulations, analysis for steady state parameters. Comparing alternative system configurations. Confidence intervals. Variance reduction techniques. Antithetic and Control variates.

Reference Books:

1. Jerry Banks, "**Discrete event system simulation"**, Pearson, 2009
2. Averill Law "**Simulation modelling and analysis"**, MGH 4th edition, 2007
3. Seila, Ceric, Tadikamalla, "**Applied simulation modelling",** Cengage, 2009.
4. George S. Fishman, "**Discrete event simulation"**, Springer, 2001
5. N. Viswanadham, Y. Narahari, "**Performance modelling of automated manufacturing systems"**, PHI, 2000
6. Frank L. Severance, "**System modelling and simulation"**, Wiley, 2009

7. K. S. Trivedi, "**Probability and statistics with reliability queuing and computer science applications",** PHI, 2007.

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III SEMESTER

COURSE CODE	16ECELPCIN	COURSE TITLE	INTERNSHIP
CREDITS	21	L-T-P-S	---

COURSE OUTCOMES

CO1	Able to develop a sound theoretical and practical knowledge of new technologies.	PO1,PO2,PO5
CO2	Able develop domain specific problem solving and critical thinking skills	PO2,PO3,PO4
CO3	Able to develop individual responsibility towards their internship goal as well as participate as an effective team member	PO6,PO7
CO4	Gain exposure to professional work culture & practices	PO9,PO10
CO5	Able to develop effective presentation & communication skills, and create proper documentation of the work	PO8,PO11

COURSE CODE	16ECELPCP1	COURSE TITLE	PROJECT WORK(I-Phase)
CREDITS	04	L-T-P-S	---

COURSE OUTCOMES

CO1	Identify a suitable project, making use of the technical and Engineering knowledge gained from previous courses with the awareness of impact of technology on the Society and their ethical responsibilities.	PO1,PO2,PO3PO4, PO5,PO9,PO10
CO2	Collect and disseminate information related to the selected project within given timeframe.	PO6,PO7
CO3	Communicate technical and general information by means of oral as well as written	PO8,PO11

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IV SEMESTER

COURSE CODE	16ECELPCP2	COURSE TITLE	PROJECT WORK(Final-Phase)
CREDITS	23	L-T-P-S	---

COURSE OUTCOMES

CO1	Identify the modern tools required for the implementation of the project.	PO5
CO2	Design, examine critically and implement or develop a prototype for the identified problem during Phase I	PO1,PO2,PO3, PO4
CO3	Communicate technical information by means of oral as well as written presentation skills with professionalism and engage in life long learning.	PO8,PO9,PO10, PO11-

COURSE CODE	16ECEL4CTS	COURSE TITLE	TECHNICAL SEMINAR
CREDITS	02	L-T-P-S	---

COURSE OUTCOMES

CO1	Identify the problem through literature survey by applying depth knowledge of the chosen domain	PO1,PO4
CO2	Analyse, synthesize and conceptualize the identified problem	PO2,PO3
CO3	Communicate clearly, write effective reports and make effective presentations following the professional code of conduct and ethics	PO8,PO10
CO4	Comprehensively study the domains and reflect the same towards the future enhancements of the work	PO11